

AVES 2019 - Technical Program

Time	December 19, 2019	December 20, 2019	December 21, 2019
08:30 am			Registration & Breakfast
09:00 am		Registration & Breakfast (6 th Floor, New CRC)	(2 nd Floor ECED New Bldg)
09:30 am	Pre-Conference Tutorial-I AGK (EC406N)	Inaugural Ceremony (Room No: 604, New CRC)	Keynote II: RKC (EC406N)
10:00 am		***Tea Break***	***Tea Break***
10:30 am	***Tea-Break***		Keynote III: RP (EC406N)
11:00 am			
11:30 am	Pre-Conference Tutorial-I AGK (EC406N)	Plenary Talk-I: GS (Room No: 604, New CRC)	Paper Presentation Sessions/ Paper ID
12:00 noon			Session II-A (EC201N) 22, 31, 32
12:30 pm			Session II-B (EC203N) 3, 26, 14
01:00 pm	***Lunch Break***	***Lunch Break***	***Lunch Break***
02:00 pm	Pre-Conference Tutorial-II VS (EC406N)	(Guest House)	(Guest House)
02:30 pm		Keynote I: VS (EC406N)	Keynote IV: HSJ (EC406N)
03:00 pm	***Tea-Break***	***Tea Break***	***Tea Break***
03:30 pm			
04:00 pm	Pre-Conference Tutorial-II VS (EC406N)	Paper Presentation Sessions/ Paper ID	Paper Presentation Sessions/ Paper ID
04:30 pm		Session I-A (EC201N) 13, 15, 16, 18, 20	Session I-B (EC203N) 12, 38, 33
05:00 pm			Session III-A (EC201N) 23, 37, 40, 44, 49
05:30 pm			Session III-B (EC203N) 17, 28, 35, 42, 50
05:30 pm	***Program Close***	***Program Close***	*** Valedictory & Conference Close***

AGK: Dr. Ashwin Kothari, VNIT, Nagpur
GS: Dr. Gaurav Sharma, University of Rochester
RP: Dr. Rutu Parekh, DAIICT, Gandhinagar

VS: Dr. Virendra Singh, IIT Bombay, Mumbai
RKC: Dr. R. K. Chauhan, MMMUT, Gorakhpur
HSJ: Shri. H. S. Jatana, SCL, S.A.S Nagar

Electronics Engineering Department
Sardar Vallabhbhai National Institute of Technology, Surat, Gujarat, India
International Conference on
"Advances in VLSI and Embedded Systems (AVES-2019)"
December 20-21, 2019

Tentative Paper Presentation Schedule

Session, Venue and Session Chair	Registration ID	Paper ID	Title	Presenting Author
Session I-A (EC201N) Anand Darji	12	13	Analysis of Memory-Based Real Fast Fourier Transform Architectures for Low-Area Applications	Rajasekhar Turaka
	20	15	Statistical Analysis of Vehicle Detection in the ITS application for monitoring the traffic and road accident using Internet of Things	Diya Naresh Vadhvani
	23	16	Gate Level Implementation and Area Optimization of SPI for Microcontroller using Structural Modeling	Mr. Amrut Anilrao Purohit
	18	18	A Novel Method of Multiplication With Ekanyunena Purvena	Mr. SAYYAD M. A.
	62	20	FPGA design of SAR type ADC based analog input module for industrial applications	G. Dhanabalan
Session I-B (EC203N) Rutu Parekh	28	12	Automated simulator for the validation of bio-impedance devices	Sruthi S.
	26	38	Smart Soldier health monitoring system incorporating embedded electronics	Mr. Parthkumar Patel
	59	33	Low Power Radix-8 Modulo 2^{n+1} Multiplier using Modified Weighted Method	Naveen Kumar Kabra
Session II-A (EC201N) Pinalkumar Engineer	57	22	The Need of Predictive Data Analytics in Cold Chain Management	Ms. Swati Dilip Kale
		31	Impact of multi-metal gate stacks on the performance of β -Ga ₂ O ₃ MOS Structure	Narendra Yadav
		32	Improved VLSI Architecture of Dual-CLCG for Pseudo-Random Bit Generator	Mangal Deep
Session II-B (EC203N)	19	3	Reusability and Scalability of an SoC Testbench in Mixed-Signal Verification - the Inevitable Necessity	Babun Chandra Pal

Virendra Singh	21	26	Test Time Reduction using Power Aware Dynamic Clock Allocation to Scan Vectors	Mr. Harikrishna Parmar
	29	14	Optimization of MEMS-Based Capacitive Sensor with High-k dielectric for Detection of Heavy Metal Ions	Dinesh Rotake
Session III-A (EC201N) Zuber Patel	53	23	FPGA Based Implementation of Artifact Suppression and Feature Extraction	Mr. Harikrishna M. Singapuri
	24	37	Image Communication using Quasi Cyclic Low Density Parity Check (QC-LDPC) code	Mr. Dharmeshkumar Jayantibhai Patel
	58	40	A 3-7 GHz CMOS Power Amplifier Design for Ultra Wide Band Applications	Dr Vishakha Purnanand Bhale
	15	44	Variability Analysis of On-Chip Interconnect System using Prospective Neural Network	Ms Ajita Misra
	13	49	Prospective Incorporation of Booster in Carbon Interconnects for High Speed Integrated Circuits	Ms. Takshashila Pathade
Session III-B (EC203N) R. K. Chauhan	35	17	Qualitative and Quantitative Analysis of Parallel Prefix Adders	Sudhanshu
	14	28	Impact of Spacers in Raised Source/Drain 14 nm technology node In _{0.53} Ga _{0.47} As-nFinFET on short channel effects	Jay Pathak
	22	35	Design of prominent single precision 32-bit floating point adder using single electron transistor operating at room temperature	Ankur Sharma
	36	42	An approach to detect and prevent Distributed Denial of Service attacks using Blockchain Technology in cloud environment	Ms. Vishwani Pankajkumar Patel
	27	50	Island Engineering of Single-Electron Transistor for Room Temperature Operation	Raj Sanjivkumar Shah

Instructions to the presenting Authors

1. Authors will be given maximum 12 minutes for power point presentation and maximum 3 minutes for question-answer session.
2. The conference venue will be equipped with a computer and LCD projector for each oral presentation room. All authors' presentations will have to be loaded in these computers before their session starts.
3. All the authors are requested to (a) visit their paper presentation venue preferably one day prior to the session, (b) verify their presentation for compatibility and proper operation. If necessary, especially if you have embedded multi-media content, you will have the final opportunity to adjust or tweak your presentation at that time.
4. We suggest the presenting author to bring his/her USB thumb drive with presentation materials in PPT/PPTX and PDF as backup.

Good Practices

- A. Try not to show more than 1 slide per minute of speaking time. This means approximately 10-12 slides MAXIMUM for the 12 minutes of presentation. Remember, the last three minutes of the presentation are for questions from the audience. USE ANIMATIONS AND SLIDE TRANSITIONS ONLY IF ABSOLUTELY NECESSARY.
- B. We recommend a slide size of 4:3 (standard).
- C. Make the letter fonts on your slides BIG ENOUGH. Suggested minimum font size is 14.
References on the slides of the body of the talk can be of font size 11.
- D. Avoid lengthy tabulations of numerical data and limit equations to those for which the terms can be properly defined.
- E. In addition to the contents of the talk, present an introduction and a summary or conclusion.
- F. If a question requires a lengthy reply, suggest that you and the person asking the question meet after the presentation. Then take the discussion out of the meeting room.